ADC1212D series

Dual 12-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps; CMOS or LVDS DDR digital outputs

Rev. 2 — 4 March 2011 Product data sheet

1. General description

The ADC1212D is a dual channel 12-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performances and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1212D is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in Complementary Metal Oxide Semiconductor (CMOS) mode, because of a separate digital output supply. It supports the Low Voltage Differential Signalling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC. The device also includes a programmable full-scale SPI to allow a flexible input voltage range of 1 V (p-p) to 2 V (p-p). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1212D is ideal for use in communications, imaging and medical applications.

2. Features and benefits

- SNR, 70 dBFS
- SFDR, 86 dBc
- Sample rate up to 125 Msps
- Clock input divided by 2 to reduce jitter contribution
- Single 3 V supply
- Flexible input voltage range: 1 V to 2 V (p-p)
- CMOS or LVDS DDR digital outputs
- Pin and software compatible with ADC1412D series and ADC1112D125.
- Input bandwidth, 600 MHz
- Power dissipation, 855 mW at 80 Msps
- Serial Peripheral Interface (SPI)
- Duty cycle stabilizer
- Fast OuT-of-Range (OTR) detection
- Offset binary, two’s complement, gray code
- Power-down and Sleep modes
- HVQFN64 package

3. Applications

- Wireless and wired broadband communications
- Portable instrumentation
- Imaging systems
- Spectral analysis
- Ultrasound equipment
- Software defined radio

4. Ordering information

Table 1. Ordering information

Type number	f_S (Msps)	Package		
		Name	Description	Version
ADC1212D125HN/C1	125	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-3
ADC1212D105HN/C1	105	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-3
ADC1212D080HN/C1	80	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-3
ADC1212D065HN/C1	65	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm	SOT804-3

5. Block diagram

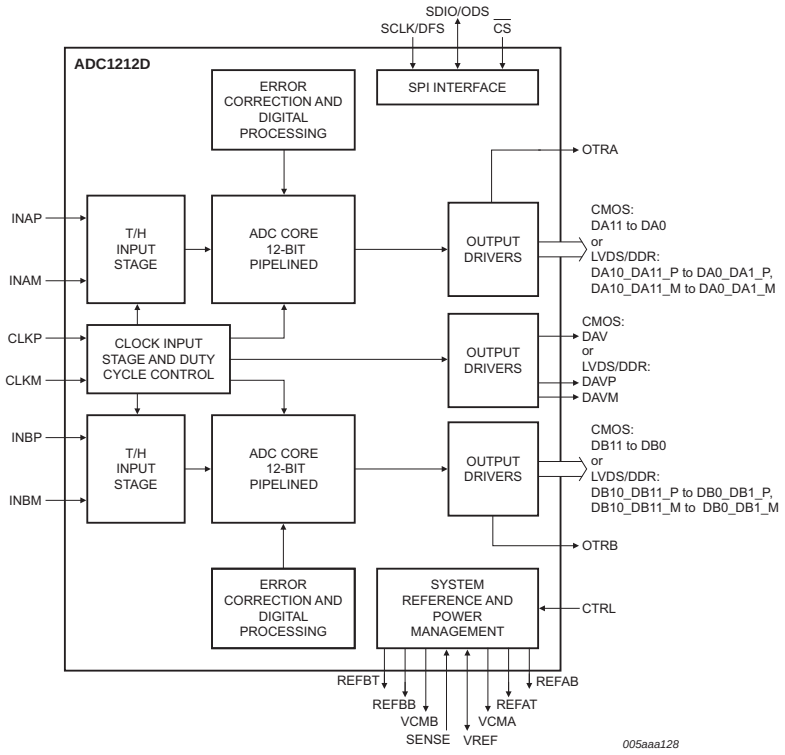

Fig 1. Block diagram

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6. Pinning information

6.1 CMOS outputs selected

6.1.1 Pinning

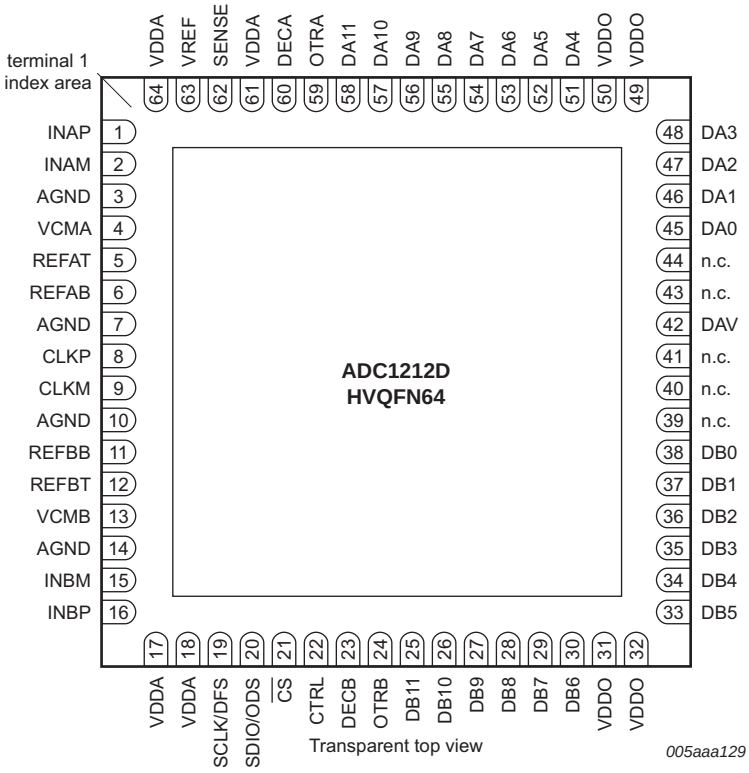

Fig 2. Pin configuration with CMOS digital outputs selected

6.1.2 Pin description

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type[1]	Description
INAP	1	I	analog input; channel A
INAM	2	I	complementary analog input; channel A
AGND	3	G	analog ground
VCMA	4	O	common-mode output voltage; channel A
REFAT	5	O	top reference; channel A
REFAB	6	O	bottom reference; channel A
AGND	7	G	analog ground
CLKP	8	I	clock input
CLKM	9	I	complementary clock input
AGND	10	G	analog ground
REFBB	11	O	bottom reference; channel B
REFBT	12	O	top reference; channel B

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Table 2. Pin description (CMOS digital outputs) *…continued*

Symbol	Pin	Type[1]	Description
VCMB	13	O	common-mode output voltage; channel B
AGND	14	G	analog ground
INBM	15	I	complementary analog input; channel B
INBP	16	I	analog input; channel B
VDDA	17	P	analog power supply
VDDA	18	P	analog power supply
SCLK/DFS	19	I	SPI clock/data format select
SDIO/ODS	20	I/O	SPI data input/output/output data standard
$\overline{CS}$	21	I	SPI chip select, active LOW
CTRL	22	I	control mode select
DECB	23	O	regulator decoupling node; channel B
OTRB	24	O	out-of-range; channel B
DB11	25	O	data output bit 11 (Most Significant Bit (MSB)); channel B
DB10	26	O	data output bit 10; channel B
DB9	27	O	data output bit 9; channel B
DB8	28	O	data output bit 8; channel B
DB7	29	O	data output bit 7; channel B
DB6	30	O	data output bit 6; channel B
VDDO	31	P	output power supply
VDDO	32	P	output power supply
DB5	33	O	data output bit 5; channel B
DB4	34	O	data output bit 4; channel B
DB3	35	O	data output bit 3; channel B
DB2	36	O	data output bit 2; channel B
DB1	37	O	data output bit 1; channel B
DB0	38	O	data output bit 0 (Least Significant Bit (LSB)); channel B
n.c.	39	-	not connected
n.c.	40	-	not connected
n.c.	41	-	not connected
DAV	42	O	data valid output clock
n.c.	43	-	not connected
n.c.	44	-	not connected
DA0	45	O	data output bit 0 (LSB); channel A
DA1	46	O	data output bit 1; channel A
DA2	47	O	data output bit 2; channel A
DA3	48	O	data output bit 3; channel A
VDDO	49	P	output power supply
VDDO	50	P	output power supply
DA4	51	O	data output bit 4; channel A
DA5	52	O	data output bit 5; channel A
DA6	53	O	data output bit 6; channel A
DA7	54	O	data output bit 7; channel A
DA8	55	O	data output bit 8; channel A
DA9	56	O	data output bit 9; channel A

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Table 2. Pin description (CMOS digital outputs) *…continued*

Symbol	Pin	Type[1]	Description
DA10	57	O	data output bit 10; channel A
DA11	58	O	data output bit 11 (MSB); channel A
OTRA	59	O	out-of-range; channel A
DECA	60	O	regulator decoupling node; channel A
VDDA	61	P	analog power supply
SENSE	62	I	reference programming pin
VREF	63	I/O	voltage reference input/output
VDDA	64	P	analog power supply

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

6.2 LVDS DDR outputs selected

6.2.1 Pinning

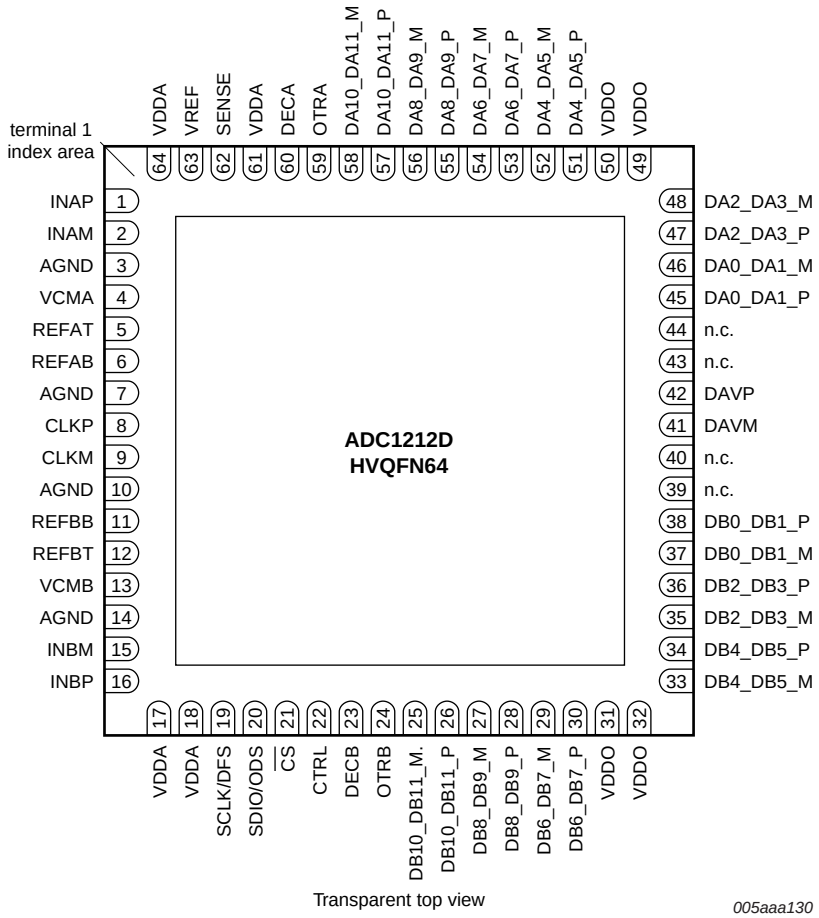

Fig 3. Pin configuration with LVDS DDR digital outputs selected

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6.2.2 Pin description

Table 3. Pin description (LVDS DDR) digital outputs)[1]

Symbol	Pin	Type[2]	Description
DB10_DB11_M	25	O	differential output data DB10 and DB11 multiplexed, complement
DB10_DB11_P	26	O	differential output data DB10 and DB11 multiplexed, true
DB8_DB9_M	27	O	differential output data DB8 and DB9 multiplexed, complement
DB8_DB9_P	28	O	differential output data DB8 and DB9 multiplexed, true
DB6_DB7_M	29	O	differential output data DB6 and DB7 multiplexed, complement
DB6_DB7_P	30	O	differential output data DB6 and DB7 multiplexed, true
DB4_DB5_M	33	O	differential output data DB4 and DB5 multiplexed, complement
DB4_DB5_P	34	O	differential output data DB4 and DB5 multiplexed, true
DB2_DB3_M	35	O	differential output data DB2 and DB3 multiplexed, complement
DB2_DB3_P	36	O	differential output data DB2 and DB3 multiplexed, true
DB0_DB1_M	37	O	differential output data DB0 and DB1 multiplexed, complement
DB0_DB1_P	38	O	differential output data DB0 and DB1 multiplexed, true
n.c.	39	-	not connected
n.c.	40	-	not connected
DAVM	41	O	data valid output clock, complement
DAVP	42	O	data valid output clock, true
n.c.	43	-	not connected
n.c.	44	-	not connected
DA0_DA1_P	45	O	differential output data DA0 and DA1 multiplexed, true
DA0_DA1_M	46	O	differential output data DA0 and DA1 multiplexed, complement
DA2_DA3_P	47	O	differential output data DA2 and DA3 multiplexed, true
DA2_DA3_M	48	O	differential output data DA2 and DA3 multiplexed, complement
DA4_DA5_P	51	O	differential output data DA4 and DA5 multiplexed, true
DA4_DA5_M	52	O	differential output data DA4 and DA5 multiplexed, complement
DA6_DA7_P	53	O	differential output data DA6 and DA7 multiplexed, true
DA6_DA7_M	54	O	differential output data DA6 and DA7 multiplexed, complement
DA8_DA9_P	55	O	differential output data DA8 and DA9 multiplexed, true
DA8_DA9_M	56	O	differential output data DA8 and DA9 multiplexed, complement
DA10_DA11_P	57	O	differential output data DA10 and DA11 multiplexed, true
DA10_DA11_M	58	O	differential output data DA10 and DA11 multiplexed, complement

[1] Pins 1 to 24, pin 59 to 64 and pins 31, 32, 49 and 50 are the same for both CMOS and LVDS DDR outputs (see Table 2).

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	output voltage	pins DA11 to DA0 and DB11 to DB0 or pins DA10_DA11_P to DA0_DA1_P, DA10_DA11_M to DA0_DA1_M, DB10_DB11_P to DB0_DB1_P and DB10_DB11_M to DB0_DB1_M	–0.4	+3.9	V
V_{DDA}	analog supply voltage		–0.4	+3.9	V
V_{DDO}	output supply voltage		–0.4	+3.9	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	15.6	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[1]	6.3	K/W

[1] Value for six layers board in still air with a minimum of 64 thermal vias.

9. Static characteristics

Table 6. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		2.85	3.0	3.4	V
V_{DDO}	output supply voltage	CMOS mode	1.65	1.8	3.6	V
		LVDS DDR mode	2.85	3.0	3.6	V
I_{DDA}	analog supply current	f_{clk} = 125 Msps; f_i = 70 MHz	-	400	-	mA
I_{DDO}	output supply current	CMOS mode; f_{clk} = 125 Msps; f_i = 70 MHz	-	16	-	mA
		LVDS DDR mode: f_{clk} = 125 Msps; f_i = 70 MHz	-	82	-	mA

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Table 6. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P	power dissipation	ADC1212D125; analog supply only	-	1230	-	mW
		ADC1212D105; analog supply only	-	1120	-	mW
		ADC1212D080; analog supply only	-	855	-	mW
		ADC1212D065; analog supply only	-	780	-	mW
		Power-down mode	-	24	-	mW
		Sleep mode	-	80	-	mW
Clock inputs: pins CLKP and CLKM						
LVPECL						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	±1.6	-	V
Sine						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	±0.8	±3.0	-	V
LVCMOS						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
Logic input: pin CTRL						
V_{IL}	LOW-level input voltage		-	0	-	V
		LOW-medium level	-	$0.3V_{DDA}$	-	V
		medium-HIGH level	-	$0.6V_{DDA}$	-	V
V_{IH}	HIGH-level input voltage		-	V_{DDA}	-	V
I_{IL}	LOW-level input current		–10	-	+10	μA
I_{IH}	HIGH-level input current		–10	-	+10	μA
Serial peripheral interface: pins $\overline{CS}$, SDIO/ODS, SCLK/DFS						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	V_{DDA}	V
I_{IL}	LOW-level input current		–10	-	+10	μA
I_{IH}	HIGH-level input current		–50	-	+50	μA
C_I	input capacitance		-	4	-	pF
Digital outputs, CMOS mode: pins DA11 to DA0, DB11 to DB0, OTRA, OTRB and DAV						
Output levels, V_{DDO}= 3 V						
V_{OL}	LOW-level output voltage		AGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DDO}$	-	V_{DDO}	V
C_O	output capacitance	high impedance; see Table 10	-	3	-	pF
Output levels, V_{DDO} = 1.8 V						
V_{OL}	LOW-level output voltage		AGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DDO}$	-	V_{DDO}	V

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Table 6. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital outputs, LVDS DDR mode: pins DA10_DA11_P to DA0_DA1_P, DA10_DA11_M to DA0_DA1_M, DB10_DB11_P to DB0_DB1_P, DB10_DB11_M to DB0_DB1_M; DAVP and DAVM						
Output levels, V_{DDO} = 3 V only, R_L = 100 Ω						
$V_{O(offset)}$	output offset voltage	output buffer current set to 3.5 mA	-	1.2	-	V
$V_{O(dif)}$	differential output voltage	output buffer current set to 3.5 mA	-	350	-	mV
C_O	output capacitance		-	3	-	pF
Analog inputs: pins INAP, INAM, INBP and INBM						
I_I	input current		–5	-	+5	μA
R_I	input resistance		-	19.8	-	kΩ
C_I	input capacitance		-	2.8	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{INAP} = V_{INAM}$; $V_{INBP} = V_{INBM}$	0.9	1.5	2	V
B_i	input bandwidth		-	600	-	MHz
$V_{I(dif)}$	differential input voltage	peak-to-peak	1	-	2	V
Common-mode output voltage: pins VCMA and VCMB						
$V_{O(cm)}$	common-mode output voltage		-	$0.5V_{DDA}$	-	V
$I_{O(cm)}$	common-mode output current		-	4	-	mA
I/O reference voltage: pin VREF						
V_{VREF}	voltage on pin VREF	output	-	0.5 to 1	-	V
		input	0.5	-	1	V
Accuracy						
INL	integral non-linearity		–1.25	±0.25	+5	LSB
DNL	differential non-linearity	guaranteed no missing codes	–0.95	±0.5	+0.95	LSB
E_{offset}	offset error		-	±2	-	mV
E_G	gain error		-	±0.5	-	%FS
$M_{G(CTC)}$	channel-to-channel gain matching		-	1.1	-	%
Supply						
PSRR	power supply rejection ratio	200 mV (p-p) on pin VDDA; f_i = DC	-	–37	-	dB

[1] Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V; $V_{INAP} - V_{INAM}$ = −1 dBFS; $V_{INBP} - V_{INBM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

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10. Dynamic characteristics

10.1 Dynamic characteristics

Table 7. Characteristics[1]

Symbol	Parameter	Conditions	ADC1212D065			ADC1212D080			ADC1212D105			ADC1212D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog signal processing															
α_{2H}	second harmonic level	f_i = 3 MHz	-	87	-	-	87	-	-	86	-	-	88	-	dBc
		f_i = 30 MHz	-	86	-	-	86	-	-	86	-	-	87	-	dBc
		f_i = 70 MHz	-	85	-	-	85	-	-	84	-	-	85	-	dBc
		f_i = 170 MHz	-	82	-	-	82	-	-	81	-	-	83	-	dBc
α_{3H}	third harmonic level	f_i = 3 MHz	-	86	-	-	86	-	-	85	-	-	87	-	dBc
		f_i = 30 MHz	-	85	-	-	85	-	-	85	-	-	86	-	dBc
		f_i = 70 MHz	-	84	-	-	84	-	-	83	-	-	84	-	dBc
		f_i = 170 MHz	-	81	-	-	81	-	-	80	-	-	82	-	dBc
THD	total harmonic distortion	f_i = 3 MHz	-	83	-	-	83	-	-	82	-	-	84	-	dBc
		f_i = 30 MHz	-	82	-	-	82	-	-	82	-	-	83	-	dBc
		f_i = 70 MHz	-	81	-	-	81	-	-	80	-	-	81	-	dBc
		f_i = 170 MHz	-	78	-	-	78	-	-	77	-	-	79	-	dBc
ENOB	effective number of bits	f_i = 3 MHz	-	11.3	-	-	11.3	-	-	11.3	-	-	11.3	-	Bits
		f_i = 30 MHz	-	11.3	-	-	11.3	-	-	11.3	-	-	11.2	-	Bits
		f_i = 70 MHz	-	11.2	-	-	11.2	-	-	11.2	-	-	11.2	-	Bits
		f_i = 170 MHz	-	11.1	-	-	11.1	-	-	11.1	-	-	11.1	-	Bits
SNR	signal-to-noise ratio	f_i = 3 MHz	-	70.0	-	-	69.9	-	-	69.8	-	-	69.6	-	dBFS
		f_i = 30 MHz	-	69.5	-	-	69.5	-	-	69.5	-	-	69.4	-	dBFS
		f_i = 70 MHz	-	69.2	-	-	69.2	-	-	69.1	-	-	69.0	-	dBFS
		f_i = 170 MHz	-	68.8	-	-	68.8	-	-	68.7	-	-	68.6	-	dBFS
SFDR	spurious-free dynamic range	f_i = 3 MHz	-	86	-	-	86	-	-	85	-	-	87	-	dBc
		f_i = 30 MHz	-	85	-	-	85	-	-	85	-	-	86	-	dBc
		f_i = 70 MHz	-	84	-	-	84	-	-	83	-	-	84	-	dBc
		f_i = 170 MHz	-	81	-	-	81	-	-	80	-	-	82	-	dBc

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Table 7. Characteristics[1] …continued

Symbol	Parameter	Conditions	ADC1212D065			ADC1212D080			ADC1212D105			ADC1212D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD	intermodulation distortion	f_i = 3 MHz	-	89	-	-	89	-	-	88	-	-	89	-	dBc
		f_i = 30 MHz	-	88	-	-	88	-	-	88	-	-	88	-	dBc
		f_i = 70 MHz	-	87	-	-	87	-	-	86	-	-	86	-	dBc
		f_i = 170 MHz	-	84	-	-	85	-	-	83	-	-	84	-	dBc
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 70 MHz	-	100	-	-	100	-	-	100	-	-	100	-	dBc

[1] Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V; $V_{INAP} - V_{INAM}$ = −1 dBFS; $V_{INBP} - V_{INBM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

10.2 Clock and digital output timing

Table 8. Clock and digital output timing characteristics[1]

Symbol	Parameter	Conditions	ADC1212D065			ADC1212D080			ADC1212D105			ADC1212D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock timing input: pins CLKP and CLKM															
f_{clk}	clock frequency		20	-	65	60	-	80	75	-	105	100	-	125	MHz
$t_{lat(data)}$	data latency time		-	14	-	-	14	-	-	14	-	-	14	-	clock cycles
δ_{clk}	clock duty cycle	DCS_EN = 1	30	50	70	30	50	70	30	50	70	30	50	70	%
		DCS_EN = 0	45	50	55	45	50	55	45	50	55	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	-	ns
t_{wake}	wake-up time		-	76	-	-	76	-	-	76	-	-	76	-	µs
CMOS mode timing: pins DA11 to DA0, DB13 to DB0 and DAV															
t_{PD}	propagation delay	DATA	-	3.9	-	-	3.9	-	-	3.9	-	-	3.9	-	ns
		DAV	-	4.2	-	-	4.2	-	-	4.2	-	-	4.2	-	ns
t_{su}	set-up time		-	8.6	-	-	7.4	-	-	6.1	-	-	5.7	-	ns
t_h	hold time		-	4.8	-	-	3.4	-	-	1.8	-	-	1.4	-	ns
t_r	rise time	DATA [2]	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
		DAV	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	ns
t_f	fall time	DATA [2]	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	0.5	-	2.4	µs

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Table 8. Clock and digital output timing characteristics[1] …continued

Symbol	Parameter	Conditions	ADC1212D065			ADC1212D080			ADC1212D105			ADC1212D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LVDS DDR mode timing: pins DA10_DA11_P to DA0_DA1_P, DA10_DA11_M to DA0_DA1_M, DB10_DB11_P to DB0_DB1_P, DB10_DB11_M to DB0_DB1_M; DAVP and DAVM															
t_{PD}	propagation delay	DATA	-	3.9	-	-	3.9	-	-	3.9	-	-	3.9	-	ns
		DAV	-	4.2	-	-	4.2	-	-	4.2	-	-	4.2	-	ns
t_{su}	set-up time		-	5.1	-	-	3.5	-	-	2.1	-	-	1.4	-	ns
t_h	hold time		-	2.0	-	-	2.0	-	-	2.0	-	-	2.0	-	ns
t_r	rise time	DATA [3]	50	100	200	50	100	200	50	100	200	50	100	200	ps
		DAV	50	100	200	50	100	200	50	100	200	50	100	200	ps
t_f	fall time	DATA [3]	50	100	200	50	100	200	50	100	200	50	100	200	ps
		DAV	50	100	200	50	100	200	50	100	200	50	100	200	ps

[1] Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, $_{Tamb}$ = 25 °C; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V; $V_{INAP} - V_{INAM}$ = −1 dBFS; $V_{INBP} - V_{INBM}$ = −1 dBFS; unless otherwise specified.

[2] Measured between 20 % to 80 % of V_{DDO}.

[3] Rise time measured from −50 mV to +50 mV; fall time measured from +50 mV to −50 mV.

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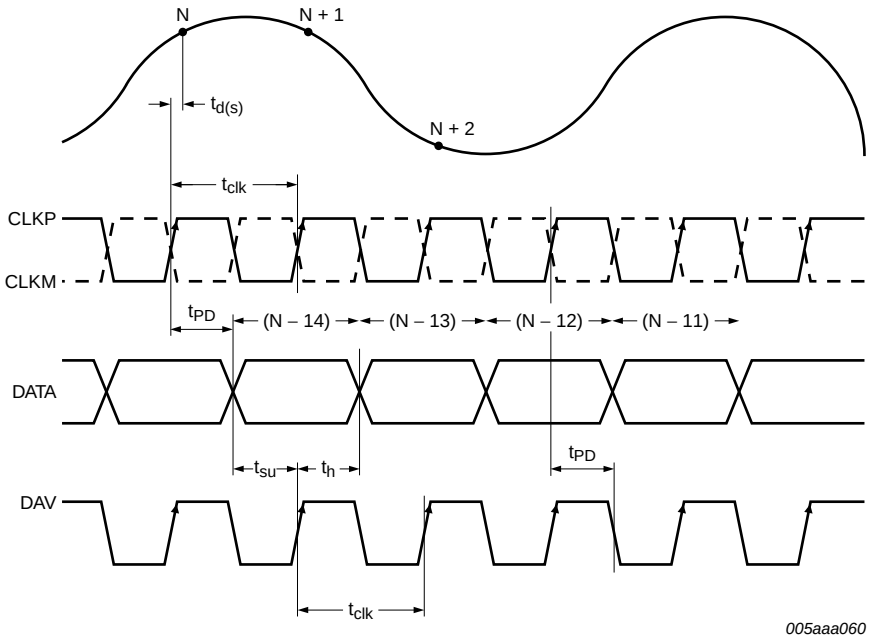
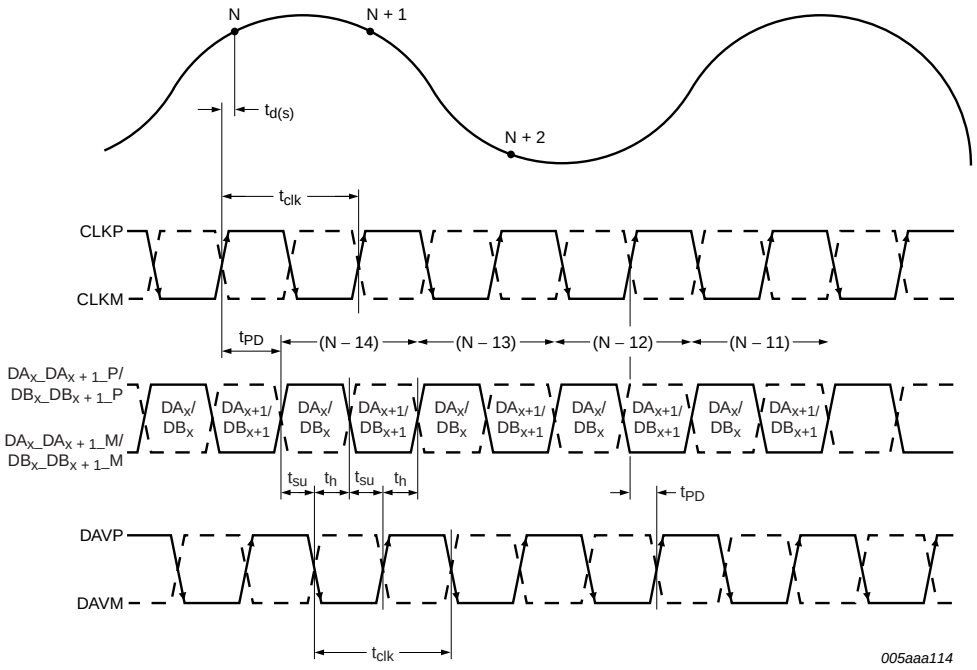


$t_{clk} = 1 / f_{clk}$

Fig 4. CMOS mode timing



$t_{clk} = 1 / f_{clk}$

Fig 5. LVDS DDR mode timing

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10.3 SPI timings

Table 9. Characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		-	40	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		-	16	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		-	16	-	ns
t_{su}	set-up time	data to SCLK HIGH	-	5	-	ns
		$\overline{CS}$ to SCLK HIGH	-	5	-	ns
t_h	hold time	data to SCLK HIGH	-	2	-	ns
		$\overline{CS}$ to SCLK HIGH	-	2	-	ns
$f_{clk(max)}$	maximum clock frequency		-	25	-	MHz

[1] Typical values measured at V_{DDA} = 3 V, V_{DDO} = 1.8 V, T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V.

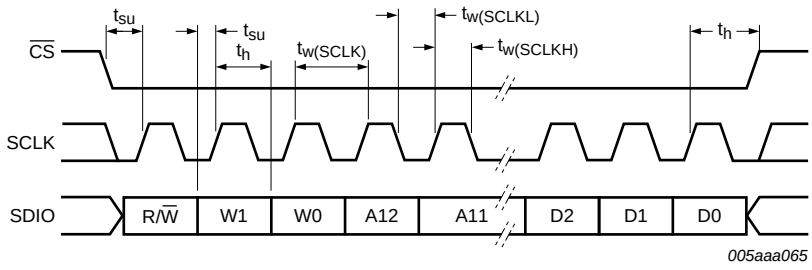

Fig 6. SPI timing

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10.4 Typical characteristics

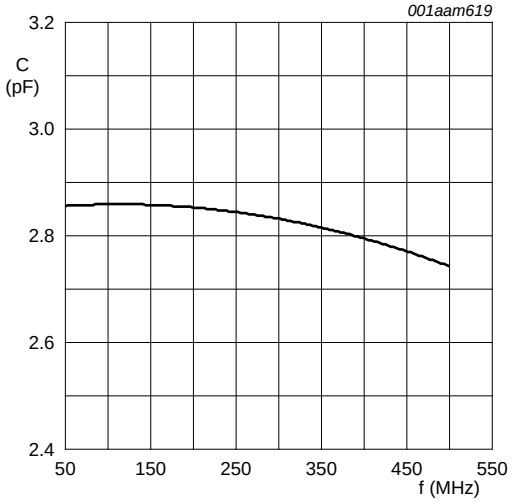


Fig 7. Capacitance as a function of frequency

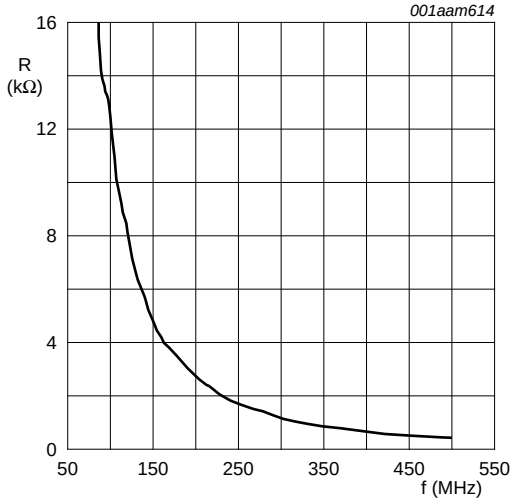
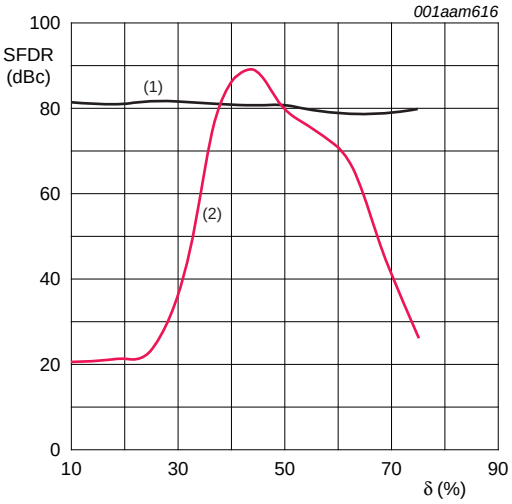


Fig 8. Resistance as a function of frequency

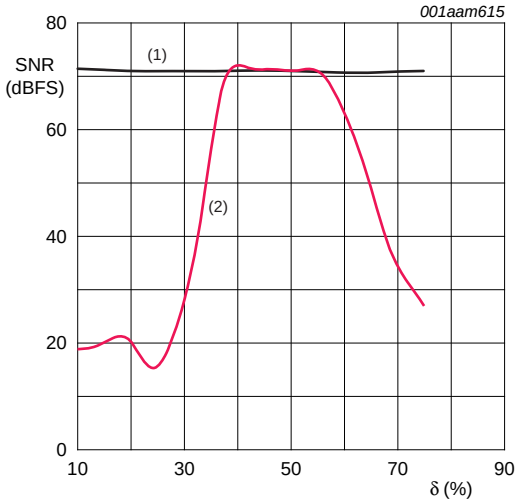


T = 25 °C; V_{DD} = 3 V; f_i = 170 MHz; f_s = 125 Msps

(1) DCS on

(2) DCS off

Fig 9. SFDR as a function of duty cycle (δ)



T = 25 °C; V_{DD} = 3 V; f_i = 170 MHz; f_s = 125 Msps

(1) DCS on

(2) DCS off

Fig 10. SNR as a function of duty cycle (δ)

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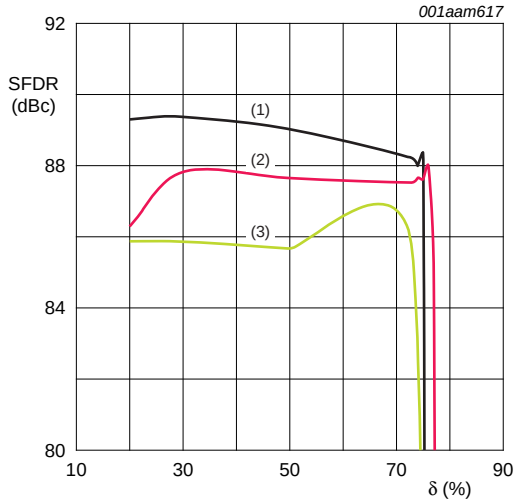
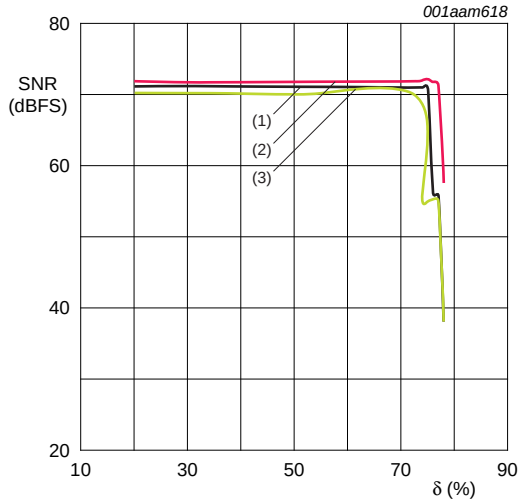


(1) T_{amb} = –40 °C/typical supply voltages
(2) T_{amb} = +25 °C/typical supply voltages
(3) T_{amb} = +90 °C/typical supply voltages

Fig 11. SFDR as a function of duty cycle (δ)



(1) T_{amb} = –40 °C/typical supply voltages
(2) T_{amb} = +25 °C/typical supply voltages
(3) T_{amb} = +90 °C/typical supply voltages

Fig 12. SNR as a function of duty cycle (δ)

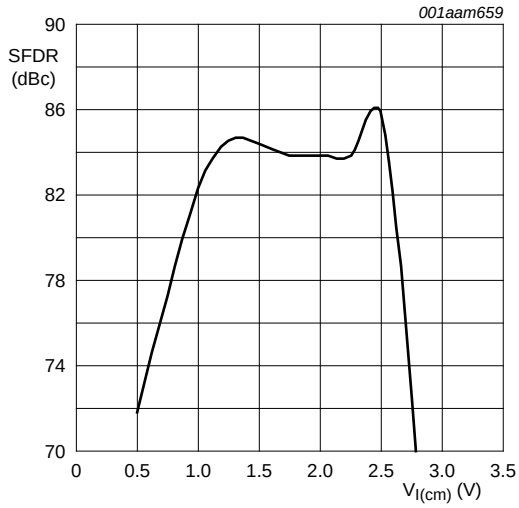


Fig 13. SFDR as a function of common-mode input voltage ($V_{I(cm)}$)

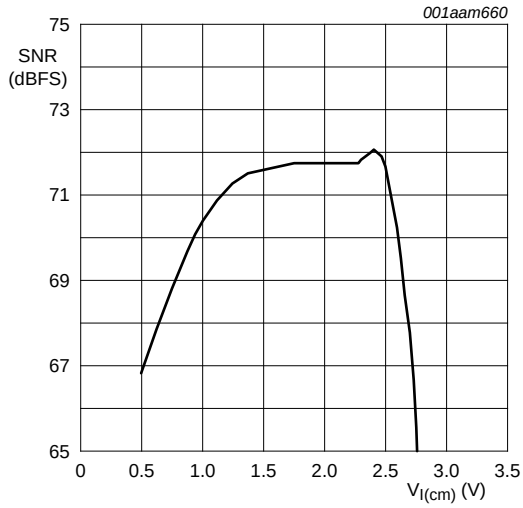


Fig 14. SNR as a function of common-mode input voltage ($V_{I(cm)}$)

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11. Application information

11.1 Device control

The ADC1212D can be controlled via the Serial Peripheral Interface (SPI control mode) or directly via the I/O pins (Pin control mode).

11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up and remains in this mode as long as pin $\overline{CS}$ is held HIGH. In Pin control mode, the SPI pins SDIO, $\overline{CS}$ and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin $\overline{CS}$ LOW. Once SPI control mode has been enabled, the device remains in this mode. The transition from Pin control mode to SPI control mode is illustrated in Figure 15.

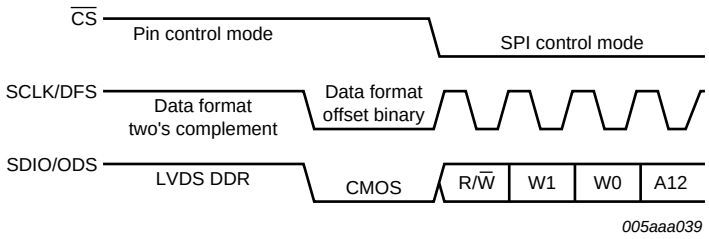

Fig 15. Control mode selection.

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO as soon as a transition is triggered by a falling edge on $\overline{CS}$.

11.1.2 Operating mode selection

The active ADC1212D operating mode (Power-up, Power-down or Sleep) can be selected via the SPI interface (see Table 21) or by using pin CTRL in Pin control mode, as described in Table 10.

Table 10. Operating mode selection via pin CTRL

Pin CTRL	Operating mode	Output high-Z
0	Power-down	yes
$0.3V_{DDA}$	Sleep	yes
$0.6V_{DDA}$	Power-up	yes
V_{DDA}	Power-up	no

11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see Table 24) or by using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

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11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two's complement or gray code; see Table 24) or by using pin DFS in Pin control mode (offset binary or two's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two's complement is selected.

11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1212D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INAP, INAM, INBP and INBM set to $0.5V_{DDA}$.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.3 and Table 23).

The equivalent circuit of the sample-and-hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics, is shown in Figure 16.

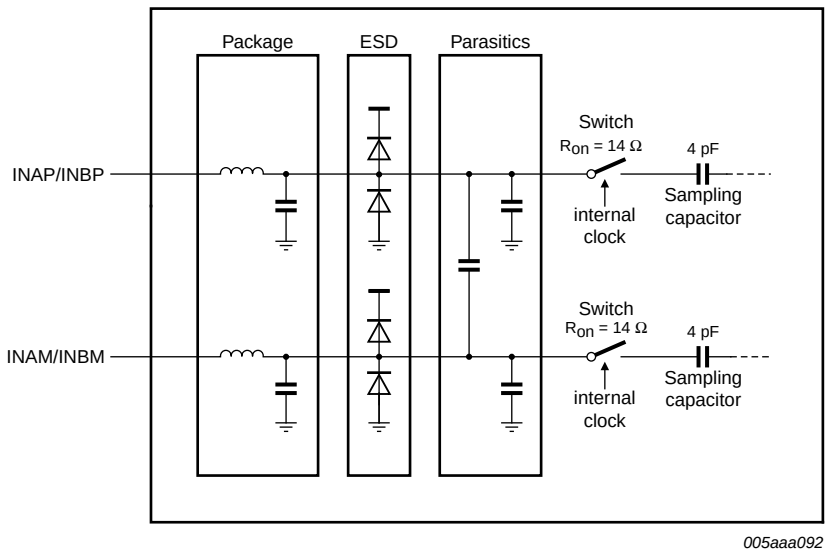

Fig 16. Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.2.2 Anti-kickback circuitry

Anti-kickback circuitry (RC filter in Figure 17 is needed to counteract the effects of charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

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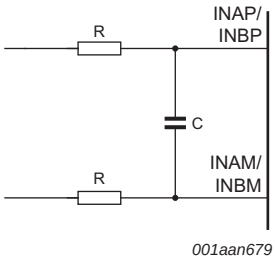

Fig 17. Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 11. RC coupling versus input frequency, typical values

Input frequency (MHz)	R (Ω)	C (pF)
3	25	12
70	12	8
170	12	8

11.2.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 18 would be suitable for a baseband application.

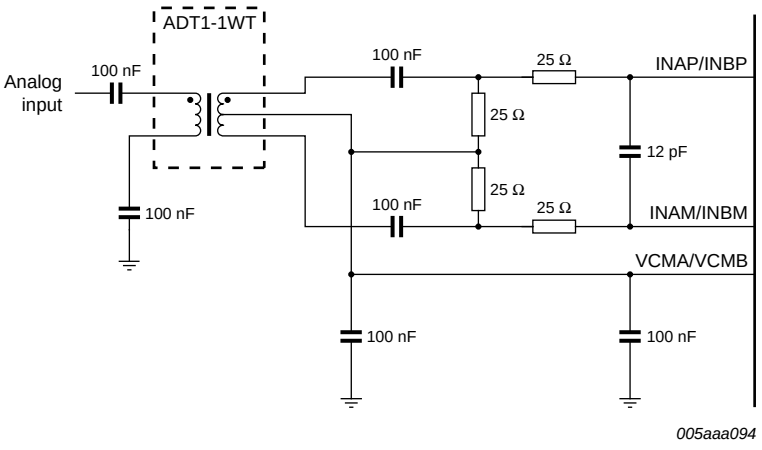

Fig 18. Single transformer configuration suitable for baseband applications

The configuration shown in Figure 19 is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

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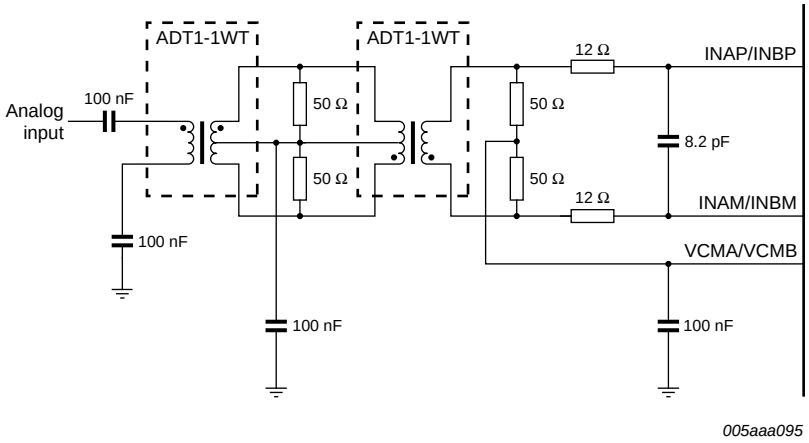

Fig 19. Dual transformer configuration suitable for high intermediate frequency application

11.3 System reference and power management

11.3.1 Internal/external references

The ADC1212D has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pin VREF and SENSE (programmable in 1 dB steps between 0 dB and −6 dB via control bits INTREF[2:0] when bit INTREF_EN = logic 1; see Table 23). See Figure 21 to Figure 24. The equivalent reference circuit is shown in Figure 20. An external reference is also possible by providing a voltage on pin VREF as described in Figure 23.

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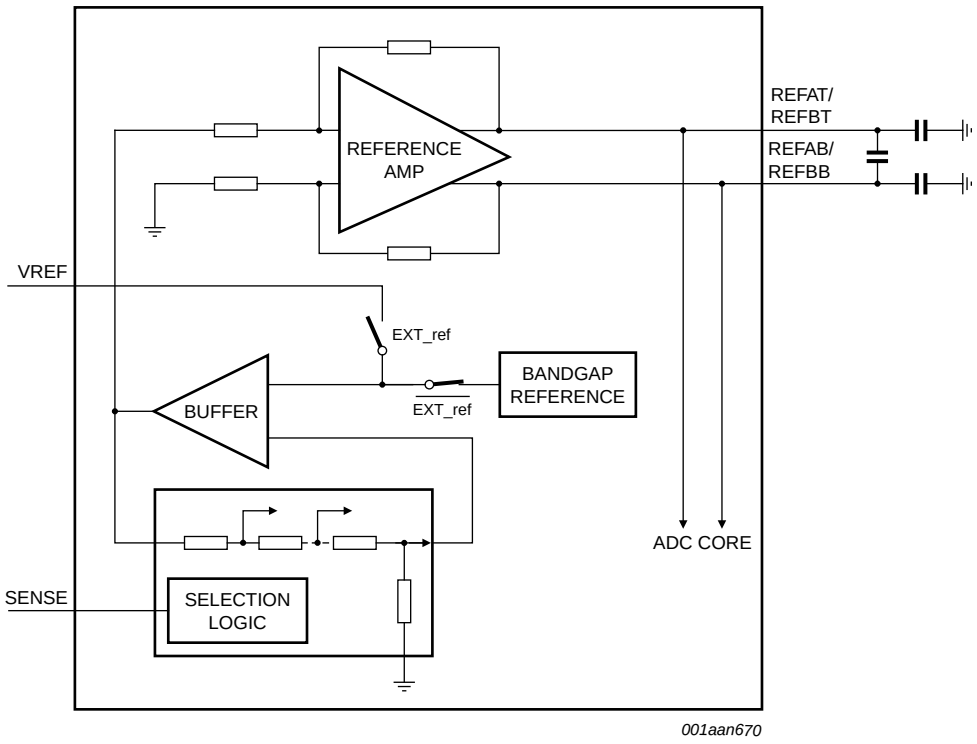

Fig 20. Reference equivalent schematic

If bit INTREF_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 12.

Table 12. Reference selection

Selection	SPI bit INTREF_EN	SENSE pin	VREF pin	Full-scale (V (p-p))
Internal (Figure 21)	0	AGND	330 pF capacitor to AGND	2 V
Internal (Figure 22)	0	pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND		1 V
External (Figure 23)	0	V_{DDA}	external voltage between 0.5 V and 1 V[1]	1 V to 2 V
Internal via SPI (Figure 24)	1	pin VREF connected to pin SENSE and via 330 pF capacitor to AGND		1 V to 2 V

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

Figure 21 to Figure 24 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

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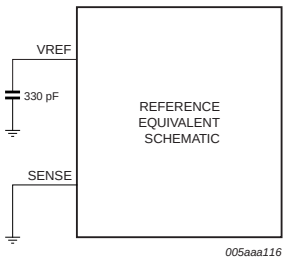

Fig 21. Internal reference, 2 V (p-p) full-scale

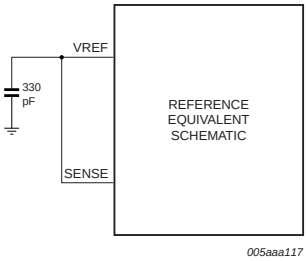

Fig 22. Internal reference, 1 V (p-p) full-scale

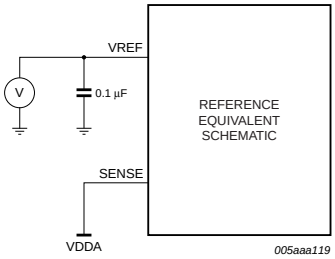

Fig 23. External reference, 1 V (p-p) to 2 V (p-p) full-scale

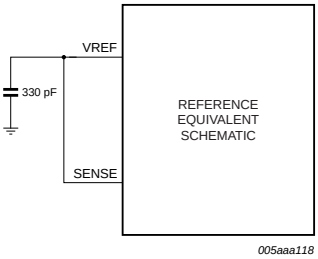

Fig 24. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale

11.3.2 Programmable full-scale

The full-scale is programmable between 1 V (p-p) to 2 V (p-p) (see Table 13).

Table 13. Programmable full-scale

INTREF	Level (dB)	Full-scale (V (p-p))
000	0	2
001	−1	1.78
010	−2	1.59
011	−3	1.42
100	−4	1.26
101	−5	1.12
110	−6	1
111	reserved	x

11.3.3 Common-mode output voltage ($V_{O(cm)}$)

A 0.1 µF filter capacitor should be connected between pin VCMA/VCMB and ground to ensure a low-noise common-mode output voltage. When AC-coupled, pin VCMA/VCMB can then be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

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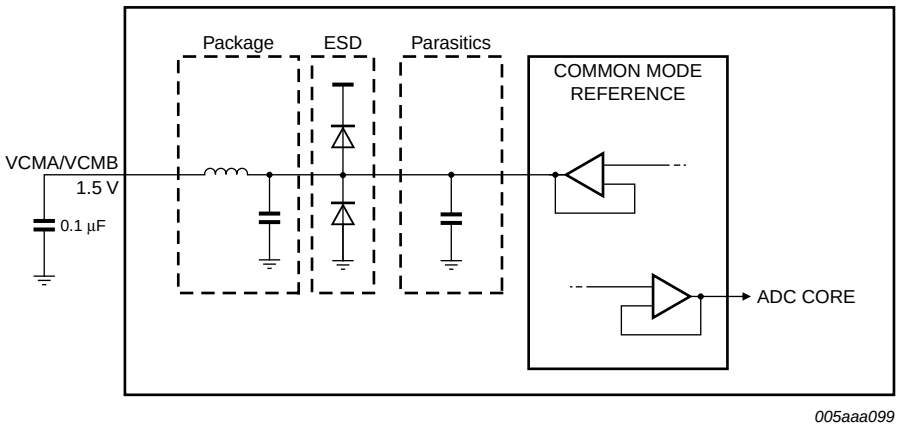


Fig 25. Equivalent schematic of the common-mode reference circuit

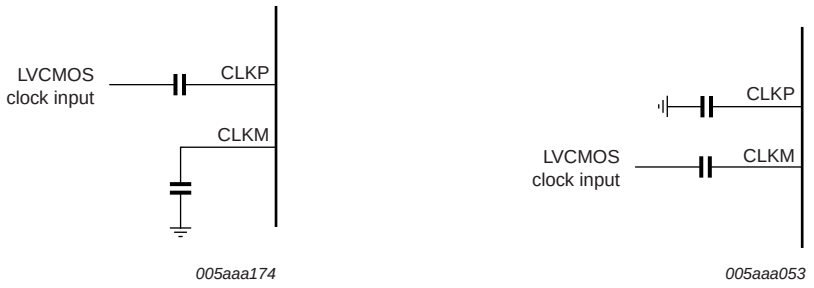
11.3.4 Biasing

The common-mode input voltage ($V_{I(cm)}$) on pins INAP/INBP and INAM/INBM should be set externally to $0.5V_{DDA}$ for optimal performance and should always be between 0.9 V and 2 V (see Table 6).

11.4 Clock input

11.4.1 Drive modes

The ADC1212D can be driven differentially (LVPECL). It can also be driven by a single-ended LVCMOS signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or pin CLKM (pin CLKP should be connected to ground via a capacitor).



a. Rising edge LVCMOS

b. Falling edge LVCMOS

Fig 26. LVCMOS single-ended clock input

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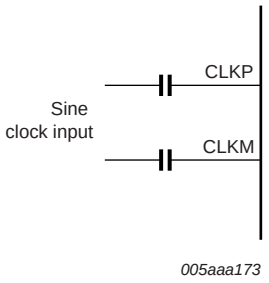
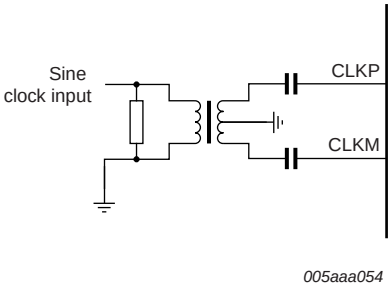
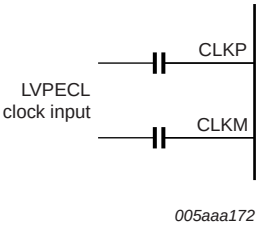


a. Sine clock input



b. Sine clock input (with transformer)

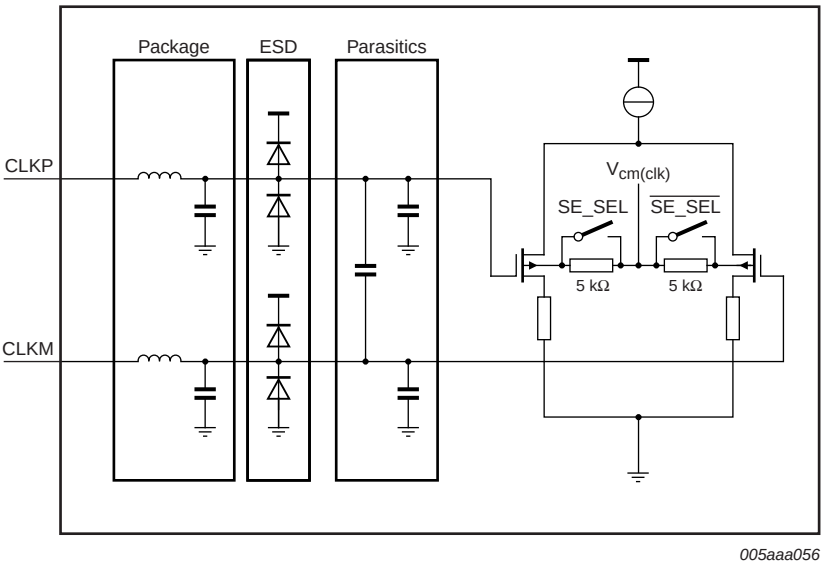


c. LVPECL clock input

Fig 27. Differential clock input

11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 28. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.



$V_{cm(clk)}$ = common-mode voltage of the differential input stage

Fig 28. Equivalent input circuit

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Single-ended or differential clock inputs can be selected via the SPI interface (see Table 22). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting bit SE_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

11.4.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS_EN = logic 1; see Table 22), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

11.4.4 Clock input divider

The ADC1212D contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = logic 1; see Table 22). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

11.5 Digital outputs

11.5.1 Digital output buffers: CMOS mode

The digital output buffers can be configured as CMOS by setting bit LVDS_CMOS to logic 0 (see Table 24).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in Figure 29. The buffer is powered by a separate AGND/V_{DDO} to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.

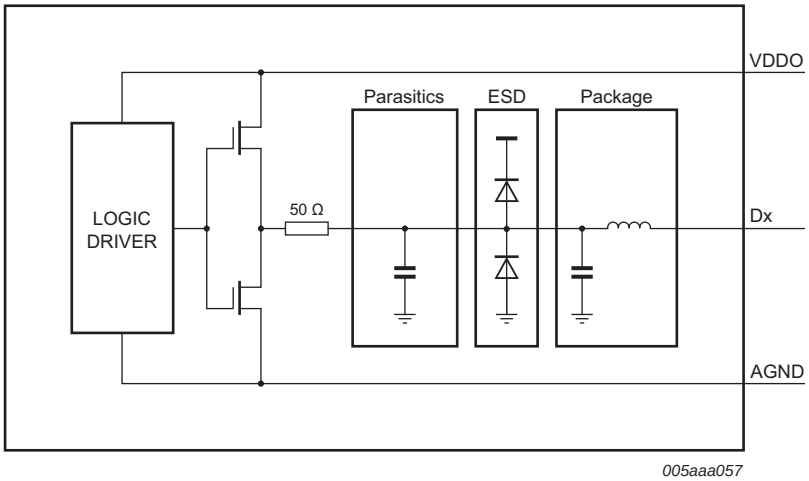

Fig 29. CMOS digital output buffer

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The output resistance is 50 Ω and is the combination of an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both DATA and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see Table 31).

11.5.2 Digital output buffers: LVDS DDR mode

The digital output buffers can be configured as LVDS DDR by setting bit LVDS_CMOS to logic 1 (see Table 24).

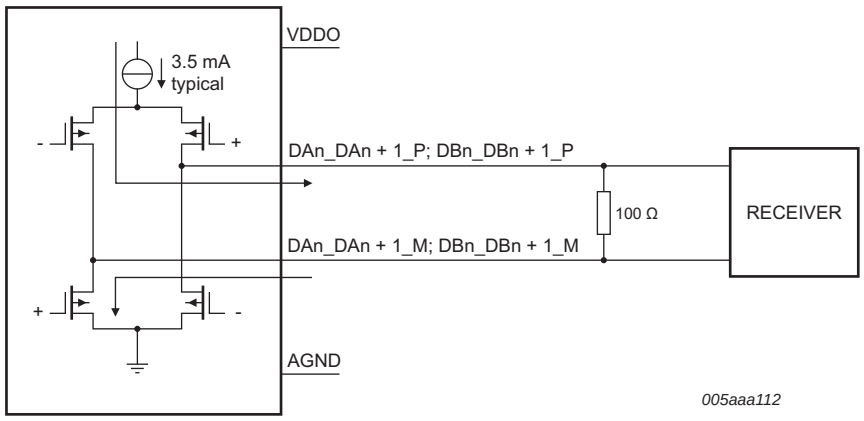

Fig 30. LVDS DDR digital output buffer - externally terminated

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side (Figure 30) or internally via SPI control bits LVDS_INT_TER[2:0] (see Figure 31 and Table 33).

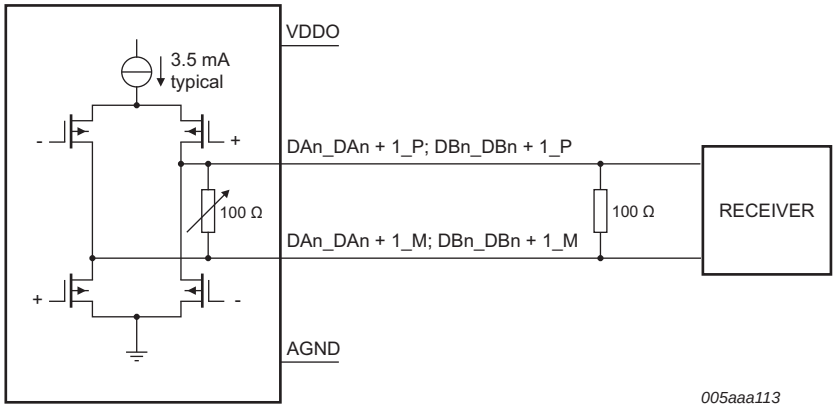

Fig 31. LVDS DDR digital output buffer - internally terminated

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI[1:0] and DATAI[1:0]; see Table 32) in order to adjust the output logic voltage levels.

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Table 14. LVDS DDR output register 2

LVDS_INT_TER[2:0]	Resistor value (Ω)
000	no internal termination
001	300
010	180
011	110
100	150
101	100
110	81
111	6

11.5.3 DAta Valid (DAV) output clock

A data valid output clock signal (DAV) is provided that can be used to capture the data delivered by the ADC1212D. Detailed timing diagrams for CMOS and LVDS DDR modes are provided in Figure 4 and Figure 5 respectively. In LVDS DDR mode, it is highly recommended to shift ahead the DAV by 1 ns (bits DAVPHASE[2:0] = 0b100; see Table 25).

11.5.4 OuT-of-Range (OTR)

An out-of-range signal is provided on pin OTRA for ADC channel A and on pin OTRB for ADC channel B. The latency of OTRA/OTRB is fourteen clock cycles. The OTR response can be speeded up by enabling Fast OTR (bit FASTOTR = logic 1; see Table 30). In this mode, the latency of OTRA/OTRB is reduced to only four clock cycles. The Fast OTR detection threshold (below full-scale) can be programmed via bits FASTOTR_DET[2:0].

Table 15. Fast OTR register

FASTOTR_DET[2:0]	Detection level (dB)
000	−20.56
001	−16.12
010	−11.02
011	−7.82
100	−5.49
101	−3.66
110	−2.14
111	−0.86

11.5.5 Digital offset

By default, the ADC1212D delivers output code that corresponds to the analog input. However, it is possible to add a digital offset to the output code via the SPI (bits DIG_OFFSET[5:0]; see Table 26).

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11.5.6 Test patterns

For test purposes, the ADC1212D can be configured to transmit one of a number of predefined test patterns (via bits TESTPAT_SEL[2:0]; see Table 27). A custom test pattern can be defined by the user (TESTPAT_USER[11:4]; see Table 28 and TESTPAT_USER[3:0]; see Table 29) and is selected when TESTPAT_SEL[2:0] = 101. The selected test pattern is transmitted regardless of the analog input.

11.5.7 Output codes versus input voltage

Table 16. Output codes

$V_{INAP} - V_{INAM}$/ $V_{INBP} - V_{INBM}$	Offset binary	Two's complement	OTRA/OTRB pin
< –1	0000 0000 0000	1000 0000 0000	1
–1.0000000	0000 0000 0000	1000 0000 0000	0
–0.9995117	0000 0000 0001	1000 0000 0001	0
–0.9990234	0000 0000 0010	1000 0000 0010	0
–0.9985352	0000 0000 0011	1000 0000 0011	0
–0.9980469	0000 0000 0100	1000 0000 0100	0
....	....	....	0
–0.0009766	0111 1111 1110	1111 1111 1110	0
–0.0004883	0111 1111 1111	1111 1111 1111	0
+0.0000000	1000 0000 0000	0000 0000 0000	0
+0.0004883	1000 0000 0001	0000 0000 0001	0
+0.0009766	1000 0000 0010	0000 0000 0010	0
....	....	....	0
+0.9980469	1111 1111 1011	0111 1111 1011	0
+0.9985352	1111 1111 1100	0111 1111 1100	0
+0.9990234	1111 1111 1101	0111 1111 1101	0
+0.9995117	1111 1111 1110	0111 1111 1110	0
+1	1111 1111 1111	0111 1111 1111	0
> +1	1111 1111 1111	0111 1111 1111	1

11.6 Serial Peripheral Interface (SPI)

11.6.1 Register description

The ADC1212D serial interface is a synchronous serial communications port that allows easy interfacing with many commonly used microprocessors. It provides access to the registers that control the operation of the chip.

This interface is configured as a 3-wire type (SDIO as bidirectional pin).

Pin SCLK is the serial clock input and $\overline{CS}$ is the chip select pin.

Each read/write operation is initiated by a LOW level on $\overline{CS}$. A minimum of three bytes is transmitted (two instruction bytes and at least one data byte). The number of data bytes is determined by the value of bits W1 and W2 (see Table 18).

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Table 17. Instruction bytes for the SPI

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/$\overline{W}$[1]	W1[2]	W0[2]	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

[1] Bit R/$\overline{W}$ indicates whether it is a read (logic 1) or a write (logic 0) operation.

[2] Bits W1 and W0 indicate the number of bytes to be transferred (see Table 18).

Table 18. Number of data bytes to be transferred after the instruction bytes

W1	W0	Number of bytes transmitted
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes or more

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is increased to access subsequent addresses.

The steps for a data transfer:

1. A falling edge on pin $\overline{CS}$ in combination with a rising edge on pin SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but is always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on pin $\overline{CS}$ indicates the end of data transmission.

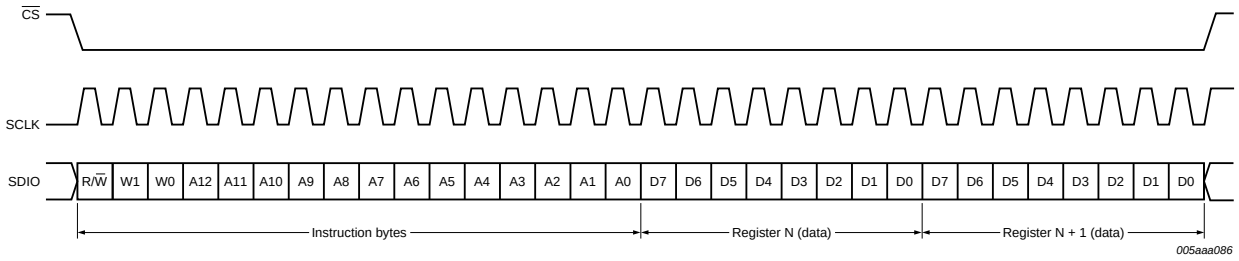

Fig 32. SPI mode timing

11.6.2 Default modes at start-up

During circuit initialization it does not matter which output data standard has been selected. At power-up, the device enters Pin control mode.

A falling edge on pin $\overline{CS}$ triggers a transition to SPI control mode. When the ADC1212D enters SPI control mode, the output data standard (CMOS/LVDS DDR) is determined by the level on pin SDIO (see Figure 33). Once in SPI control mode, the output data standard can be changed via bit LVDS_CMOS (see Table 24).

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When the ADC1212D enters SPI control mode, the output data format (two's complement or offset binary) is determined by the level on pin SCLK (gray code can only be selected via the SPI). Once in SPI control mode, the output data format can be changed via bit DATA_FORMAT[1:0] (see Table 24).

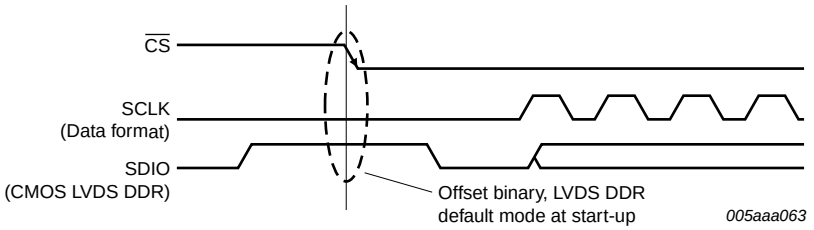

Fig 33. Default mode at start-up: SCLK LOW = offset binary; SDIO HIGH = LVDS DDR

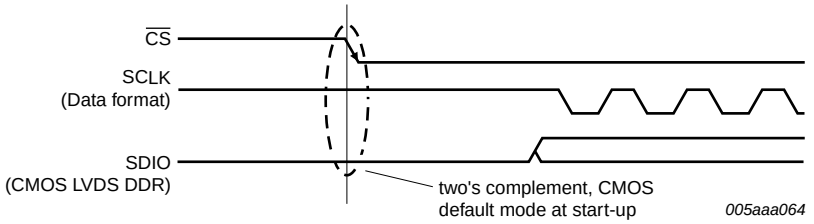

Fig 34. Default mode at start-up: SCLK HIGH = two's complement; SDIO LOW = CMOS

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11.6.3 Register allocation map

Table 19. Register allocation map

Addr (hex)	Register name	Access	Bit definition								Default (bin)
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0003	Channel index	R/W	RESERVED[5:0]						ADCB	ADCA	1111 1111
0005	Reset and operating mode	R/W	SW_RST	RESERVED[2:0]			-	-	OP_MODE[1:0]		0000 0000
0006	Clock	R/W	-	-	-	SE_SEL	DIFF_SE	-	CLKDIV	DCS_EN	0000 0001
0008	Internal reference	R/W	-	-	-	-	INTREF_EN	INTREF[2:0]			0000 0000
0011	Output data standard.	R/W	-	-	-	LVDS_CMOS	OUTBUF	OUTBUS_SWAP	DATA_FORMAT[1:0]		0000 0000
0012	Output clock	R/W	-	-	-	-	DAVINV	DAVPHASE[2:0]			0000 1110
0013	Offset	R/W	-	-	DIG_OFFSET[5:0]						0000 0000
0014	Test pattern 1	R/W	-	-	-	-	-	TESTPAT_SEL[2:0]			0000 0000
0015	Test pattern 2	R/W	TESTPAT_USER[11:4]								0000 0000
0016	Test pattern 3	R/W	TESTPAT_USER[3:0]				-	-	-	-	0000 0000
0017	Fast OTR	R/W	-	-	-	-	FASTOTR	FASTOTR_DET[2:0]			0000 0000
0020	CMOS output	R/W	-	-	-	-	DAV_DRV[1:0]		DATA_DRV[1:0]		0000 1110
0021	LVDS DDR O/P 1	R/W	-	-	RESERVED	DAVI[1:0]		RESERVED	DATAI[1:0]		0000 0000
0022	LVDS DDR O/P 2	R/W	-	-	-	-	BIT_BYTE_WISE	LVDS_INT_TER[2:0]			0000 0000

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Table 20. Channel index control register (address 0003h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 2	RESERVED[5:0]	-	**111111**	reserved
1	ADCB	R/W		next SPI command for ADC B
			0	ADC B not selected
			1	ADC B selected
0	ADCA	R/W		next SPI command for ADC A
			0	ADC A not selected
			1	ADC A selected

Table 21. Reset and operating mode control register (address 0005h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7	SW_RST	R/W		reset digital section
			0	**no reset**
			1	performs a reset on SPI registers
6 to 4	RESERVED[2:0]	-	**000**	reserved
3 to 2	-	-	00	not used
1 to 0	OP_MODE[1:0]	R/W		operating mode
			00	**normal (Power-up)**
			01	Power-down
			10	Sleep
			11	normal (Power-up)

Table 22. Clock control register (address 0006h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-	-	000	not used
4	SE_SEL	R/W		single-ended clock input pin select
			0	**CLKM**
			1	CLKP
3	DIFF_SE	R/W		differential/single-ended clock input select
			0	**fully differential**
			1	single-ended
2	RESERVED	-	0	reserved
1	CLKDIV	R/W		clock input divide by 2
			0	**disabled**
			1	enabled
0	DCS_EN	R/W		duty cycle stabilizer
			0	disabled
			1	**enabled**

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Table 23. Internal reference control register (address 0008h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3	INTREF_EN	R/W		programmable internal reference enable
			0	**disable**
			1	active
2 to 0	INTREF[2:0]	R/W		programmable internal reference
			000	**0 dB (FS = 2 V)**
			001	−1 dB (FS = 1.78 V)
			010	−2 dB (FS = 1.59 V)
			011	−3 dB (FS = 1.42 V)
			100	−4 dB (FS = 1.26 V)
			101	−5 dB (FS = 1.12 V)
			110	−6 dB (FS = 1 V)
			111	reserved

Table 24. Output data standard control register (address 0011h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	-	-	000	not used
4	LVDS_CMOS	R/W		output data standard: LVDS DDR or CMOS
			0	**CMOS**
			1	LVDS DDR
3	OUTBUF	R/W		output buffers enable
			0	**output enabled**
			1	output disabled (high Z)
2	OUTBUS_SWAP	R/W		output bus swap
			0	**no swapping**
			1	output bus is swapped (MSB becomes LSB and vice versa)
1 to 0	DATA_FORMAT[1:0]	R/W		output data format
			00	**offset binary**
			01	two’s complement
			10	gray code
			11	offset binary

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Table 25. Output clock register (address 0012h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3	DAVINV	R/W		output clock data valid (DAV) polarity
			0	normal
			1	**inverted**
2 to 0	DAVPHASE[2:0]	R/W		DAV phase select
			000	output clock shifted (ahead) by 6/16 × t_{clk}[1]
			001	output clock shifted (ahead) by 5/16 × t_{clk}[1]
			010	output clock shifted (ahead) by 4/16 × t_{clk}[1]
			011	output clock shifted (ahead) by 3/16 × t_{clk}[1]
			100	output clock shifted (ahead) by 2/16 × t_{clk}[1]
			101	output clock shifted (ahead) by 1/16 × t_{clk}[1]
			110	**default value as defined in timing section**
			111	output clock shifted (delayed) by 1/16 × t_{clk}[1]

[1] $t_{clk} = 1 / f_{clk}$

Table 26. Offset register (address 0013h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	-	-	00	not used
5 to 0	DIG_OFFSET[5:0]	R/W		digital offset adjustment
			011111	+31 LSB
			...	...
			000000	**0**
			...	...
			100000	−32 LSB

Table 27. Test pattern register 1 (address 0014h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 3	-	-	00000	not used
2 to 0	TESTPAT_SEL[2:0]	R/W		digital test pattern select
			000	**off**
			001	mid scale
			010	−FS
			011	+FS
			100	toggle ‘1111..1111’/’0000..0000’
			101	custom test pattern
			110	‘0101..0101’
			111	‘1010..1010.’

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Table 28. Test pattern register 2 (address 0015h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	TESTPAT_USER[11:4]	R/W	**0000 0000**	**custom digital test pattern (bits 11 to 4)**

Table 29. Test pattern register 3 (address 0016h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	TESTPAT_USER[3:0]	R/W	**0000**	**custom digital test pattern (bits 3 to 0)**
3 to 0	-	-	0000	not used

Table 30. Fast OTR register (address 0017h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3	FASTOTR	R/W		fast OuT-of-Range (OTR) detection
			0	**disabled**
			1	enabled
2 to 0	FASTOTR_DET[2:0]	R/W		set fast OTR detect level
			000	**−20.56 dB**
			001	−16.12 dB
			010	−11.02 dB
			011	−7.82 dB
			100	−5.49 dB
			101	−3.66 dB
			110	−2.14 dB
			111	−0.86 dB

Table 31. CMOS output register (address 0020h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3 to 2	DAV_DRV[1:0]	R/W		drive strength for DAV CMOS output buffer
			00	low
			01	medium
			10	high
			11	**very high**
1 to 0	DATA_DRV[1:0]	R/W		drive strength for DATA CMOS output buffer
			00	low
			01	medium
			10	**high**
			11	very high

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Table 32. LVDS DDR output register 1 (address 0021h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	-	-	00	not used
5	RESERVED	-	0	**reserved**
4 to 3	DAVI[1:0]	R/W		LVDS current for DAV LVDS buffer
			00	**3.5 mA**
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA
2	RESERVED	-	0	reserved
1 to 0	DATAI[1:0]	R/W		LVDS current for DATA LVDS buffer
			00	**3.5 mA**
			01	4.5 mA
			10	1.25 mA
			11	2.5 mA

Table 33. LVDS DDR output register 2 (address 0022h) bit description

Default values are highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	-	-	0000	not used
3	BIT_BYTE_WISE	R/W		DDR mode for LVDS output
			0	**bit wise (even data bits output on DAV rising edge/odd data bits output on DAV falling edge)**
			1	byte wise (MSB data bits output on DAV rising edge/LSB data bits output on DAV falling edge)
2 to 0	LVDS_INT_TER[2:0]	R/W		internal termination for LVDS buffer (DAV and DATA)
			000	**no internal termination**
			001	300 Ω
			010	180 Ω
			011	110 Ω
			100	150 Ω
			101	100 Ω
			110	81 Ω
			111	60 Ω

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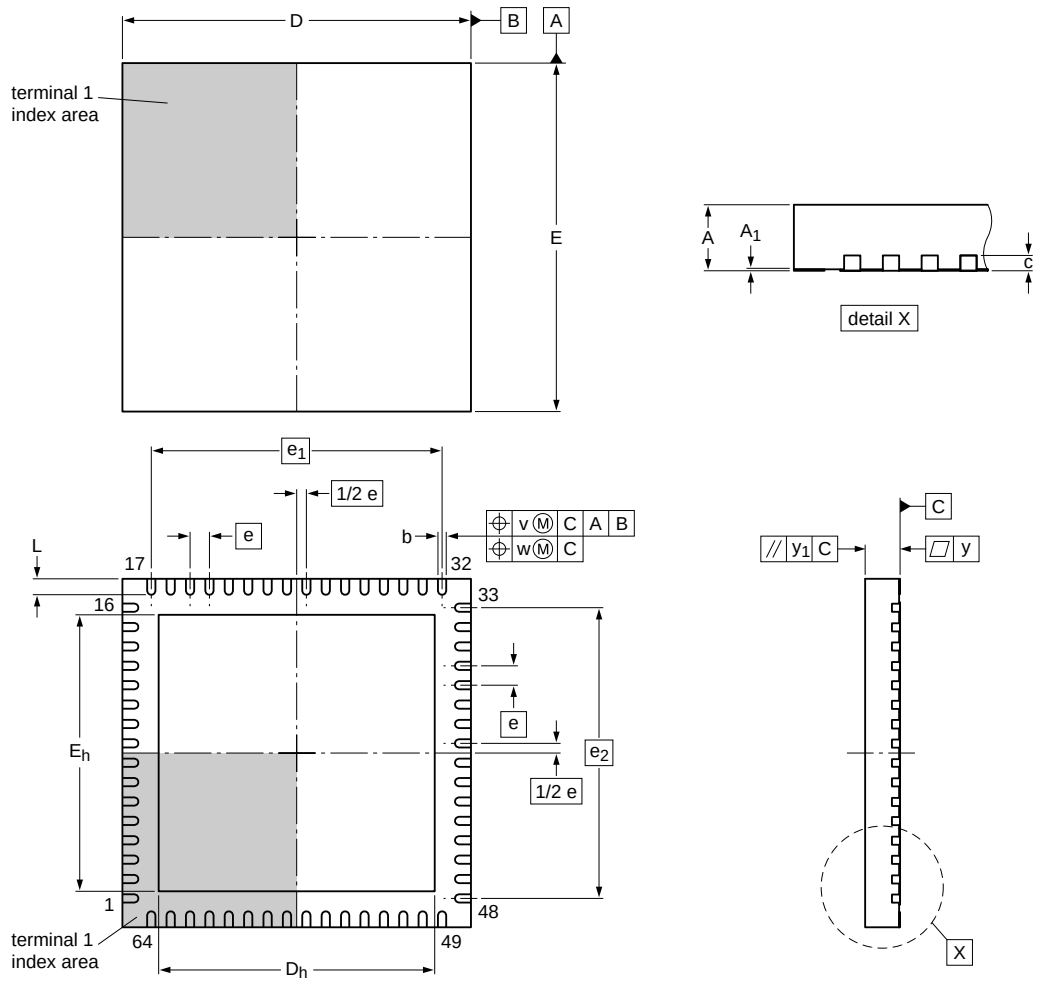
12. Package outline

HVQFN64: plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 x 9 x 0.85 mm **SOT804-3**



Dimensions

Unit		A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		9.1	7.25	9.1	7.25				0.5				
mm	nom	0.85	0.02	0.21	0.2	9.0	7.10	9.0	7.10	0.5	7.5	7.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		8.9	6.95	8.9	6.95				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot804-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT804-3	- - -	- - -	- - -			~~09-02-24~~ 10-08-06

Fig 35. Package outline SOT804-3 (HVQFN64)

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13. Abbreviations

Table 34. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
DAV	DAta Valid
DCS	Duty Cycle Stabilizer
DFS	Data Format Select
ESD	ElectroStatic Discharge
FS	Full-Scale
IMD	InterModulation Distortion
LSB	Least Significant Bit
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS DDR	Low Voltage Differential Signalling Double Data Rate
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
MSB	Most Significant Bit
OTR	OuT-of-Range
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TX	Transmitter

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14. Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1212D_SER v.2	20110304	Product data sheet	-	ADC1212D_SER v.1
Modifications:	• Data sheet status changed from Preliminary to Product. • Text and drawings updated throughout entire data sheet. • Section 10.4 “Typical characteristics” has been added to the data sheet. • Section 13 “Abbreviations” has been added to the data sheet.			
ADC1212D_SER v.1	20100806	Preliminary data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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